

App. Serial No. 10/534,655
Docket No.: DE 020249 US

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In the Claims:

Please amend claims 1-7 as indicated below. This listing of claims replaces all prior versions.

1. (*Currently Amended*) A phase comparator[[,]] providing regulating signals for a PLL module, and that compares ~~the~~ a phase angle of a first input signal with a second input signal by evaluating ~~the~~ edges of the first and the second input signals and generates reset signals therefrom using a circuit, characterized in that at least one additional circuit is provided that further evaluates ~~further~~, different edges of the first input signal or the second input signals and generates therefrom additional reset signals, wherein for the each of the reset signals and each of the additional reset signals reset the regulating signal ~~or~~ signals.
2. (*Currently Amended*) A phase comparator as claimed in claim 1, characterized in that the phase comparator obtains the regulating signals from ~~the~~ rising[[f]] and decaying edges of the first and the second input signals and in that the at least one additional circuit derives the additional reset signals from the ~~decaying/rising~~ rising and decaying edges of the first and the second input signals.
3. (*Currently Amended*) A phase comparator as claimed in claim 1, characterized in that a dedicated additional circuit is provided for each of the ~~two~~ first and the second input signals, with one of the dedicated additional circuits evaluating the edges of the first input signal and the ~~second~~ other dedicated additional circuit evaluating the edges of the second input signal.
4. (*Currently Amended*) A phase comparator as claimed in claim 1, characterized in that ~~one~~ another additional circuit evaluates ~~the~~ rising and decaying edges of one of the first and the second input signals and the ~~other~~ at least one additional circuit evaluates ~~the~~ rising and decaying edges of the other input signal.

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5. (*Currently Amended*) A phase comparator as claimed in claim 1, characterized in that the output signals from the at least one additional circuit[[s]] are applied to the reset inputs of flip-flops belonging to the phase comparator via a gate, there also being connected to the gate a gate to which the regulating signals are applied.

6. (*Currently Amended*) A phase comparator as claimed in claim 1, characterized in that the at least one additional circuit[[s]] ~~each have~~ has two RS flip-flops and gates, which are integrated into the PLL circuit module.

7. (*Currently Amended*) A phase comparator as claimed in claim 1, characterized in that the ~~two~~ first and the second input signals are applied to the at least one additional circuit via an OR gate.